IN THE CLAIMS

Listing of Claims:

1. (currently amended) An apparatus for managing operations in a processor, said apparatus comprising:

a plurality of addressable registers, each of said registers partitioned into plurality of data entry fields;

a first comparison circuit~~, said first comparison circuit~~ operable to scan a like data entry field of said plurality of addressable registers and compare [[a]] data ~~value~~ in ~~a set of~~ said like data entry fields to [[a]] predetermined input data~~ value~~;

a second comparison circuit~~, said second comparison circuit~~ operable to compare a first register address of a first register in said plurality of addressable registers~~, corresponding to a comparison match of said first comparison circuit,~~ to a second register address of a second register in said plurality of addressable registers, wherein said first register address corresponds to a first register that has said data in said like data entry field that matches said predetermined input data; and

a dispatch circuit operable to dispatch data of a second data entry field of [[a]] said second register ~~corresponding to said second register address~~ to an operation unit in response to a decode of data in a third data entry field of said second register ~~and a comparison match of~~ when said second comparison circuit indicates said second register matches said first register address.

2. (original) The apparatus of claim 1, wherein said operations are Load and Store operations within said processor.

3. (currently amended) The apparatus of claim 1, wherein said predetermined input ~~value~~ data is a real address requesting particular data corresponding to one of a Load and a Store operation.

4. (previously presented) The apparatus of claim 1, wherein said first comparison circuit comprises multiple like entry comparison circuits, each of said multiple like entry comparison circuits operable concurrently in parallel.

5. (original) The apparatus of claim 1, wherein said operation unit comprises an Instruction Management Unit (IMU).

6. (previously presented) The apparatus of claim 2, wherein said operation unit comprises a Storage Management Unit (SMU) said SMU comprising data cache memory and controller and a Storage Reference Buffer (SRB).

7. (original) The apparatus of claim 1, wherein one of said data entry fields is a Valid bit field, said Valid bit field indicating whether other data entry fields are valid.

8. (original) The apparatus of claim 1, wherein one of said data entry fields is an Instruction Identification (ID) field corresponding to a particular Load and Store operation.

9. (original) The apparatus of claim 1, wherein one of said data entry fields is an Instruction status field corresponding to a status of one of said Load and Store operations.

10. (original) The apparatus of claim 1, wherein one of said data entry fields is a Load/Store field having a Load/Store bit, said Load/Store bit corresponding to a Load operation if said Load/Store bit has a first logic state and corresponding to a Store operation if said Load/Store bit has a second logic state.

11. (original) The apparatus of claim of claim 1, wherein one of said data entry fields comprises Real Address field, said Real Address field corresponding to a particular Real Address of memory data.

12. (original) The apparatus of claim 1, wherein one of said data entry fields is a Quadword field, said Quadword field comprising multiple bytes of data.

13. (original) The apparatus of claim 1, wherein one of said data entry fields is an Operand Mask field, said Operand Mask field defining selected bytes of data within a selected one of said data entry fields.

14. (original) The apparatus of claim 1, wherein said operation unit is a pipeline execution unit operating concurrently on a plurality of said data entry fields.

15. (original) The apparatus of claim 1, wherein said addressable registers are addressed using a plurality of address pointers.

16. (previously presented) The apparatus of claim 6 wherein said addressable registers are configured as said Storage Reference Buffer (SRB).

17. (original) The apparatus of claim 15, wherein one of said address pointers is a third pointer, said third pointer, said third pointer pointing to one of said addressable registers whose data entry fields contain data defining an earliest Store operation that is either unresolved or that matches a register address of a current Load operation.

18. (original) The apparatus of claim 15, wherein said address pointers comprise a fourth and a fifth pointer, said fourth and fifth pointers defining a window of register addresses from which a Load operation may be satisfied without having to access other memory storage.

19. (original) The apparatus of claim 15, wherein said second register address is selected from registers addresses which fall within a window of register addresses, said window of addresses defined by said address pointers.

20. (original) The apparatus of claim 15, wherein one of said address pointers is a first pointer, said first pointer pointing to an IN register address of a first available register into which data may be added.

21. (original) The apparatus of claim 15, wherein one of said address pointers is a second pointer, said second pointer pointing to an OUT register address of a first available register from which register data may be retired.

22. (original) The apparatus of claim 16, wherein said data entry fields, added to said SRB after a mis-predicted branch instruction occurs in said processor, are retired and said first pointer is indexed to first register address of a register with added register data entry bits which were added immediately prior to said mis-predicted branch instruction.

23. (original) The apparatus of claim 19, wherein said window of register addresses defines active Load and Store operations.

24. (original) The apparatus of claim 20, wherein said first pointer is indexed by one when said register data has been added, said first pointer having a minimum and a maximum value wherein a decrement down from a minimum value results in said maximum value and an increment up from said maximum value results in said minimum value.

25. (original) The apparatus of claim 21, wherein said second pointer is indexed by one when register entry bits have been deleted, said second pointer having a minimum and a maximum value wherein a decrement down from said minimum value results in said maximum value and an increment up from said maximum value results in said minimum value.

26. (currently amended) A data processing system, comprising:

a central processing unit (CPU);

random access memory (RAM);

read only memory (ROM);

an I/O adapter; and

a bus system coupling devices internal to said CPU, said CPU comprising an apparatus for managing operations within a processor of said CPU, said apparatus comprising:

a first comparison circuit~~, said first comparison circuit~~ operable to scan a like data entry field of said plurality of addressable registers and compare [[a]] data ~~value~~ in ~~a set of~~ said like data entry fields to [[a]] predetermined input data ~~value~~;

a second comparison circuit~~, said second comparison circuit~~ operable to compare a first register address of a first register in said plurality of addressable registers~~, corresponding to a comparison match of said first comparison circuit,~~ to a second register address of a second register in said plurality of addressable registers, wherein said first register address corresponds to a first register that has said data in said like data entry field that matches said predetermined input data; and

a dispatch circuit operable to dispatch data of a second data entry field of [[a]] said second register ~~corresponding to said second register address~~ to an operation unit in response to a decode of data in a third data entry field of said second register ~~and a comparison match of~~ when said second comparison circuit indicates said second register matches said first register address.

27. (original) The data processing system of claim 26, wherein said operations are Load and Store operations within said processor.

28. (currently amended) The data processing system of claim 26, wherein said predetermined input ~~value~~ data is a real address requesting particular data corresponding to one of a Load and a Store operation.

29. (previously presented) The data processing system of claim 26, wherein said first comparison circuit comprises multiple like entry comparison circuits, each of said multiple like entry comparison circuits operable concurrently in parallel.

30. (original) The data processing system of claim 26, wherein said operation unit comprises an Instruction Management Unit (IMU).

31. (previously presented) The data processing system of claim 27, wherein said operation unit comprises a Storage Management Unit (SMU) said SMU comprising data cache memory and controller and a Storage Reference Buffer (SRB).

32. (original) The data processing system of claim 26, wherein one of said data entry fields is a Valid bit field, said Valid bit field indicating whether other data entry fields are valid.

33. (original) The data processing system of claim 26, wherein one of said data entry fields is an Instruction Identification (ID) field corresponding to a particular Load and Store operation.

34. (original) The data processing system of claim 26, wherein one of said data entry fields is an Instruction status field corresponding to a status of one of said Load and Store operations.

35. (original) The data processing system of claim 26, wherein one of said data entry fields is a Load/Store field having a Load/Store bit, said Load/Store bit corresponding to a Load operation if said Load/Store bit has a first logic state and corresponding to a Store operation if said Load/Store bit has a second logic state.

36. (original) The data processing system of claim of claim 26, wherein one of said data entry fields comprises Real Address field, said Real Address field corresponding to a particular Real Address of memory data.

37. (original) The data processing system of claim 26, wherein one of said data entry fields is a Quadword field, said Quadword field comprising multiple bytes of data.

38. (original) The data processing system of claim 26, wherein one of said data entry fields is an Operand Mask field, said Operand Mask field defining selected bytes of data within a selected one of said data entry fields.

39. (original) The data processing system of claim 26, wherein said operation unit is a pipeline execution unit operating concurrently on a plurality of said data entry fields.

40. (original) The data processing system of claim 26, wherein said addressable registers are addressed using a plurality of address pointers.

41. (previously presented) The data processing system of claim [[26]] 31 wherein said addressable registers are configured as said Storage Reference Buffer (SRB).

42. (original) The data processing system of claim 40, wherein one of said address pointers is a third pointer, said third pointer, said third pointer pointing to one of said addressable registers whose data entry fields contain data defining an earliest Store operation that is either unresolved or that matches a register address of a current Load operation.

43. (original) The data processing system of claim 40, wherein said address pointers comprise a fourth and a fifth pointer, said fourth and fifth pointers defining a window of register addresses from which a Load operation may be satisfied without having to access other memory storage.

44. (original) The data processing system of claim 40, wherein said second register address is selected from registers addresses which fall within a window of register addresses, said window of addresses defined by said address pointers.

45. (original) The data processing system of claim 40, wherein one of said address pointers is a first pointer, said first pointer pointing to an IN register address of a first available register into which data may be added.

46. (original) The data processing system of claim 40, wherein one of said address pointers is a second pointer, said second pointer pointing to an OUT register address of a first available register from which register data may be retired.

47. (original) The data processing system of claim 41, wherein said data entry fields, added to said SRB after a mis-predicted branch instruction occurs in said processor, are retired and said first pointer is indexed to first register address of a register with added register data entry bits which were added immediately prior to said mis-predicted branch instruction.

48. (original) The data processing system of claim 44, wherein said window of register addresses defines active Load and Store operations.

49. (original) The data processing system of claim 45, wherein said first pointer is indexed by one when said register data has been added, said first pointer having a minimum and a maximum value wherein a decrement down from a minimum value results in said maximum value and an increment up from said maximum value results in said minimum value.

50. (original) The data processing system of claim 46, wherein said second pointer is indexed by one when register entry bits have been deleted, said second pointer having a minimum and a maximum value wherein a decrement down from said minimum value results in said maximum value and an increment up from said maximum value results in said minimum value.

55. (previously presented) The apparatus of claim 6, wherein the SRB comprises the plurality of addressable registers.

56. (previously presented) The apparatus of claim 55, wherein a Load operation in one of the Load and Store operations comprises:

issuing concurrently a fetch instruction requesting a real address to a data cache and the Storage Reference Buffer (SRB), the real address corresponding to an address of multiple bytes of data;

scanning the addressable registers in the SRB for the real address;

receiving the multiple bytes of data from the SRB if the real address is available;

retrieving the multiple bytes of data first from the SRB if the real address is available and second from the data cache if the real address is not available in the SRB; and

updating a corresponding one of the addressable registers with the multiple bytes of data.

57. (previously presented) The apparatus of claim 55, wherein a Store operation in one of the Load and Store operations comprises:

issuing a real address generation instruction;

looking up the real address in a table lookup buffer;

sending the real address to a miss resolution processor if the real address is not in the table lookup buffer, the miss resolution processor determining a translated real address;

sending the real address from one of the miss resolution processors and the table lookup buffer to the SRB; and

updating corresponding data entry fields in one of the addressable registers in the SRB.

58. (previously presented) The apparatus of claim 55, wherein a Store operation in one of the Load and Store operations comprises:

issuing an address generation instruction by a first instruction unit generating a real address in memory;

updating the real address in a real address field of one of the addressable registers in the SRB;

sending concurrently, a request for a multiple byte word with the real address to the SRB and a data cache;

receiving the multiple byte word from one of the addressable registers in the Storage Reference Buffer and from a data cache;

updating the multiple byte word from the data cache with an operand mask;

receiving from the first instruction unit store data operand;

aligning the store data operand to the multiple bytes of data; and

updating the multiple bytes of data with a complement of the operand mask.

59. (previously presented) The apparatus of claim 55, wherein a Load operation in one of the Load and Store operations comprises:

issuing an address generation instruction by a first instruction unit generating a real address in a memory;

updating the real address in a real address field of one of the addressable registers in the SRB;

sending concurrently, a request for a multiple byte word with the real address to the SRB and a data cache;

receiving the multiple byte word from one of the addressable registers in the SRB and the data cache;

extracting selected bytes from the multiple byte word;

receiving the selected bytes by the first instruction unit; and

updating the multiple bytes of data with a complement of the operand mask.